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In re application of: Devries, C. et al.

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Filed: July 28, 2003 | Examiner: TBD

Title: POWER DOWN SYSTEM AND METHOD FOR INTEGRATED CIRCUITS

SUBMISSION OF PRIORITY DOCUMENT

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Alexandria, VA 22313-1450

Dear Sir:

Enclosed is a copy of Canadian Priority Document No. 2,393,651 for the above-described application. Accordingly, the claim for priority under 35 U.S.C.§ 119 is satisfied.

It is believed that no fee is required. If any additional fees are required, the Commissioner is authorized to charge Deposit Account No. 13-2165.

Respectfully submitted,

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DATE: July 28, 2003

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Certification

This is to certify that the documents attached hereto and identified below are true copies of the documents on file in the Patent Office.

Specification and Drawing, as originally filed, with Application for Patent Serial No: **2,393,651,** on July 29, 2002, by **RALPH DICKSON MASON, CHRISTOPHER ANDREW DEVRIES and THEODORE PANTAZOPOULOS,** for "Low Power Oscillator and Power Down Method".

L. Régimbal

Agent certificateur/Certifying Officer

June 25, 2003

Date

FILE NO. PRIVILEGED AND CONFIDENTIAL

Title

Low Power Oscillator and Power Down Method

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Abstract

A low power Oscillator Circuit and a method for using this oscillator in a power down mode is taught herein. The power down method (Figure 1) is accomplished by turning off a crystal oscillator (1) and standard circuitry (2) and using only the low power relaxation oscillator (3) and realtime counters that are part of the oscillator control circuit (4). To provide precision timing while in power down mode, the oscillator frequency of the low power relaxation oscillator (3) is measured in standard operating mode by the oscillator control circuit (4) using the precision crystal oscillator (1) as a reference frequency. By accurately measuring the low power relaxation oscillator (3) frequency, the length of the power down time can be programmed using a real time counter in the oscillator control circuit (4). Furthermore, when exiting from power down mode, the oscillator control circuit can use a second real time counter to first turn on the crystal oscillator (1) and let it stabilize before turning on the standard circuitry (2). Furthermore, after precisely measuring the low power relaxation oscillator (3) frequency, the low power relaxation oscillator (3) and oscillator control circuit (4) is used to precisely measure the crystal oscillator (1) power up time and adjust crystal oscillator (1) bias currents to optimize power consumption versus crystal oscillator (1) power-up time.

Field of the Invention

The invention relates to Integrated Circuits (ICs) with power down mode. In particular, it relates to ICs that require a timed power down mode in which the power consumption of the ICs is reduced to a minimum.

Background of the Invention

Many integrated circuit systems have a power down mode that is used to save power and in the case of battery operated systems, extend the battery life of the system. Exit from power down mode is usually controlled by an external interrupt signal or is preprogrammed for a fixed time. The latter case is most common in stand alone systems where an IC must wake up at know intervals to perform a function such as monitor sensors or communicate with other devices.

When an IC is required to wake up at know intervals, then during the power down mode some circuitry needs to be operating to keep track of time. This circuitry usually includes some type of oscillator and real time counter. In many cases the oscillator frequency needs to be accurately know, and possibly adjusted, over a wide range of operating conditions. A common solution is to use a crystal oscillator that has a very precise and temperature insensitive oscillator frequency. However, to guarantee proper operation, a crystal oscillator will usually require tens of μA (10^{-6} Amps) of bias current.

Low cost Integrated Circuit (IC) oscillators such as ring oscillators and relaxation oscillators are required for many applications and have been implement in wide variety of systems (e.g. U.S. Pat. No. 6,404,690 issued June 11, 2002, U.S. Pat. No. 6,388,479 issued May 14, 2002, U.S. Pat. No. 6,219,797 issued April 17, 2001). A major limitation with these oscillators is that their frequency of oscillation is not precisely know. It has been proposed that these low cost oscillators could be made programmable to adjust their frequency (U.S. Pat. No. 6,377,129 issued April 23, 2002). It has also been proposed that to save power an IC could use both a precise crystal oscillator and a standard ring oscillator whereby the ring oscillator could be used when the crystal oscillator is powering up and still not stable (U.S. Pat. No. 6,219,797 issued April 17, 2001). These previous embodiments are principally aimed at replacing high

cost oscillators with low cost oscillators that do not require an expensive crystal. In one case, (U.S. Pat. No. 6,219,797 issued April 17, 2001), the low cost oscillator is used to save power during the power-up of the crystal oscillator.

Summary of the Invention

There is therefore provided in a present embodiment of the invention a method for saving power in an IC during power down mode. First, the oscillation frequency of a specially designed low power oscillator is measured. The IC is then put in power down mode for a precise amount of time as measured by the low power oscillator and a real time counter. The IC is then powered up and normal operation using the crystal oscillator is resumed. To further save power, the power up time of the crystal oscillator is optimized by measuring the power up time with the low power oscillator and adjusting the bias currents in the crystal oscillator. The low power oscillator is implemented as a special relaxation oscillator. The oscillator is a Schmitt trigger with programmable frequency, limited power dissipation and power down control.

The methods claimed herein provide an extremely low power or standby current for the IC when compared to that of a system where a crystal oscillator is kept on in power down. The power of the crystal oscillator is also minimized in startup due to the control by the low power oscillator. The apparatuses claimed herein enable the use of this low power – power down method. The relaxation oscillator claimed herein provides lower power, controlled operation than other IC oscillators.

Description of the Drawings

Many of the features and advantages of the present invention will be better understood from the following detailed description read in light of the accompanying drawings, wherein

Figure 1 Illustrates a block diagram of the system

Figure 2 Illustrates a circuit diagram of the specially designed low power relaxation oscillator

Figure 3 Illustrates a timing diagram of the system showing power consumption

Figure 4 Illustrates a flow diagram of the power down operation

Detailed Description of the Preferred Embodiments

The present invention now will be described more fully with reference to the accompanying drawings, in which embodiments of the invention are shown. Those skilled in the art will appreciate that the invention may be embodied in many different forms and should not be construed as limited to the embodiments set forth herein; rather, these embodiments are provided so that this disclosure will be thorough and complete, and will fully convey the scope of the invention to those skilled in the art. In the drawings, like numbers refer to like elements throughout.

For purposes of the discussion herein, descriptions of preferred embodiments utilizing low power relaxation oscillator for power down mode power saving are provided. Those skilled in the art will appreciate, however, that the present invention need not be limited to relaxation

oscillators. It will be understood that in general, any low power IC oscillators may be used with the present invention.

The present invention arises from the realization that a current limited relaxation oscillator (or other low power IC oscillator) can operate on much less current than a crystal oscillator. The drawback with using a relaxation oscillator is that the frequency of oscillator is not well controlled and is dependent on environmental conditions. To overcome this limitation a method of achieving a low power - power down mode is claimed. The method consists of combining the functionality of a crystal oscillator (1), low power relaxation oscillator (3) and oscillator control circuit (4) (Figure 1).

The power down method is accomplished by turning off the crystal oscillator (1) and standard circuitry (2) and using only the low power relaxation oscillator (3) and real time counters (5) that are part of the oscillator control circuit. To provide precision timing while in power down mode, the oscillator frequency of the low power relaxation oscillator (3) is measured in standard operating mode by the oscillator control circuit (4) using the precision crystal oscillator (1) as a reference frequency. By accurately measuring the low power relaxation oscillator (3) frequency, the length of the power down time can be programmed using a real time counter (5) in the oscillator control circuit (4). Furthermore, when exiting from power down mode, the oscillator control circuit (4) can use a second real time counter (5) to first turn on the crystal oscillator (1) and let it stabilize before turning on the standard circuitry (2). Furthermore, after precisely measuring the low power relaxation oscillator frequency, the low power relaxation oscillator (3) and oscillator control circuit (4) can be used to precisely measure the crystal oscillator power up time and adjust crystal oscillator bias currents to optimize power consumption versus crystal oscillator power-up time.

A timing diagram showing the basic operation can be seen in figure 3. There are three basic modes of operation: power down mode (10), power up crystal oscillator mode (12) and power up standard circuitry mode (14). During power down mode (10) only the relaxation oscillator (3) and oscillator control circuit (4) are operating. This mode has the lowest power consumption. During power up crystal oscillator mode (12) the crystal oscillator (1) is turned on in addition to the relaxation oscillator (3) and oscillator control circuit (4) and the total power consumption is increased. During power up crystal oscillator mode (12) the crystal oscillator starts oscillating and reaches stable oscillation near the end of this mode (16). In power up standard circuitry mode (14) the standard operating circuits (2) of the IC are turned on in addition to the crystal oscillator (1), oscillator control circuit (4) and relaxation oscillator (3). This mode consumes the largest total power. During power up standard circuitry mode (14) the relaxation oscillator (3) may optionally be turned off to reduce noise and power.

A flow graph describing the basic operation of the system can be seen in Figure 4. After resetting the system (40), the standard circuitry (2) sends a power down signal (42) and the oscillator control circuitry (4) measures the output frequency of the low power oscillator (44). The IC then enters power down mode (46). It remains in power down mode (46) for a preprogrammed period of time and then enters power up crystal oscillator mode (48) again for a preprogrammed period of time until the crystal oscillator is stable. The IC then enters power up standard circuitry mode (50). After the IC performs the necessary functions (52), the power down signal is again asserted (42) by the standard circuitry and the cycle is repeated.

A low power relaxation relaxation oscillator (Figure 2) can be realized using a Schmitt trigger configuration (M22-M29) whose currents are limited by the current sources formed by

transistors M16-M19. The current in transistors M16-M19 is determined by an input bias current (Ibias) that is mirrored in transistors M1, M16 and M17. The frequency of oscillation is determined by the charging time of capacitor C1 that is charged by a programmable current mirror formed by transistors M2-M15 with input current from Ibias and M1. The feedback path for the oscillator connects the output (Out) to the charging capacitor C1 through transistors M30 and M31 and capacitor C2. The low power relaxation oscillator can be shut down by turning off transistor M30, thereby breaking the feedback path.

While the present invention has been illustrated and described with reference to specific embodiments, further modifications and improvements will occur to those skilled in the art. It is to be understood, therefore, that this invention is not limited to the particular forms illustrated, for example, other types of oscillators could be used, and that it is intended to cover all modifications that do not depart from the spirit and scope of this invention.

Claims

We claim :

1. A method for providing a power down mode to an IC, the method comprising:

(a) Precisely measuring the frequency of oscillation of a low power oscillator using a high precision oscillator

(b) Shutting down the standard circuitry and high precision oscillator

(c) Counting the time interval since power down using the low power oscillator clock signal and the measured frequency of said oscillator

(d) Powering up the high precision oscillator at a predetermined, programmable time delay

(e) Powering up the standard circuitry after oscillation in the precision oscillator is stabilized

2. A method for minimizing the power up current of a crystal oscillator, the method comprising:

(a) The precise measurement of a low power oscillator output frequency using a high precision oscillator

(b) Powering down the crystal oscillator

(c) Starting up the crystal oscillator

(d) Measuring the startup time and optimizing the amount of power used by the crystal oscillator during startup, based on the maximum required power up time for the crystal oscillator.

3. An apparatus comprising of:

(a) Standard circuitry, said standard circuitry is configurable in a powered-up state and a powered-down state

(b) A crystal oscillator circuit for outputting a precision clock signal, said crystal oscillator circuit is configurable in a powered-up state and a powered-down state

(c) A low power oscillator circuit for outputting a second clock signal

(d) An oscillator control circuit that is able to power down and power up the crystal oscillator circuit and standard circuitry

(e) A real time counter and control circuits to measure the low power oscillator frequency during the powered-up state using the crystal oscillator output as a reference signal, to measure the length of time for the powered-down state and to start up the crystal oscillator at a predetermined time and let it stabilize before powering-up the standard circuitry

4. An apparatus, as described in claim 3 comprising of:

(a) A control circuit to regulate the power used by the crystal oscillator in startup mode, such that the power is optimized for the required oscillator startup time, as measured by the real time counter in claim 3 (e).

5. A low power relaxation oscillator circuit comprising:

(a) a Schmitt trigger circuit whose current supply is limited by a set of four current sources.

(b) a programmable current mirror for charging a capacitor and thereby setting the fundamental frequency of the relaxation oscillator

(c) an external bias current and current mirror for setting the bias levels in the low power relaxation oscillator.

(d) a feedback path that can be turned off or turned on to either shut down or power up the low power relaxation oscillator

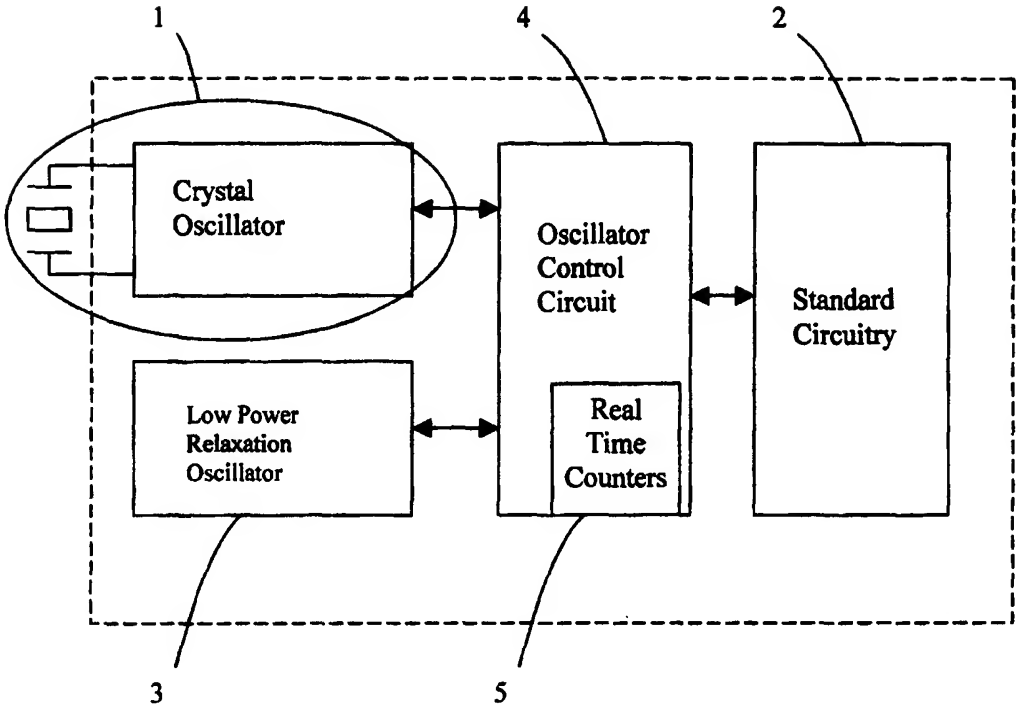
1
4
2
Crystal
Oscillator
Oscillator
Control
Circuit
Standard
Circuitry
Low Power
Relaxation
Oscillator
Real
Time
Counters
3
5

Figure 1

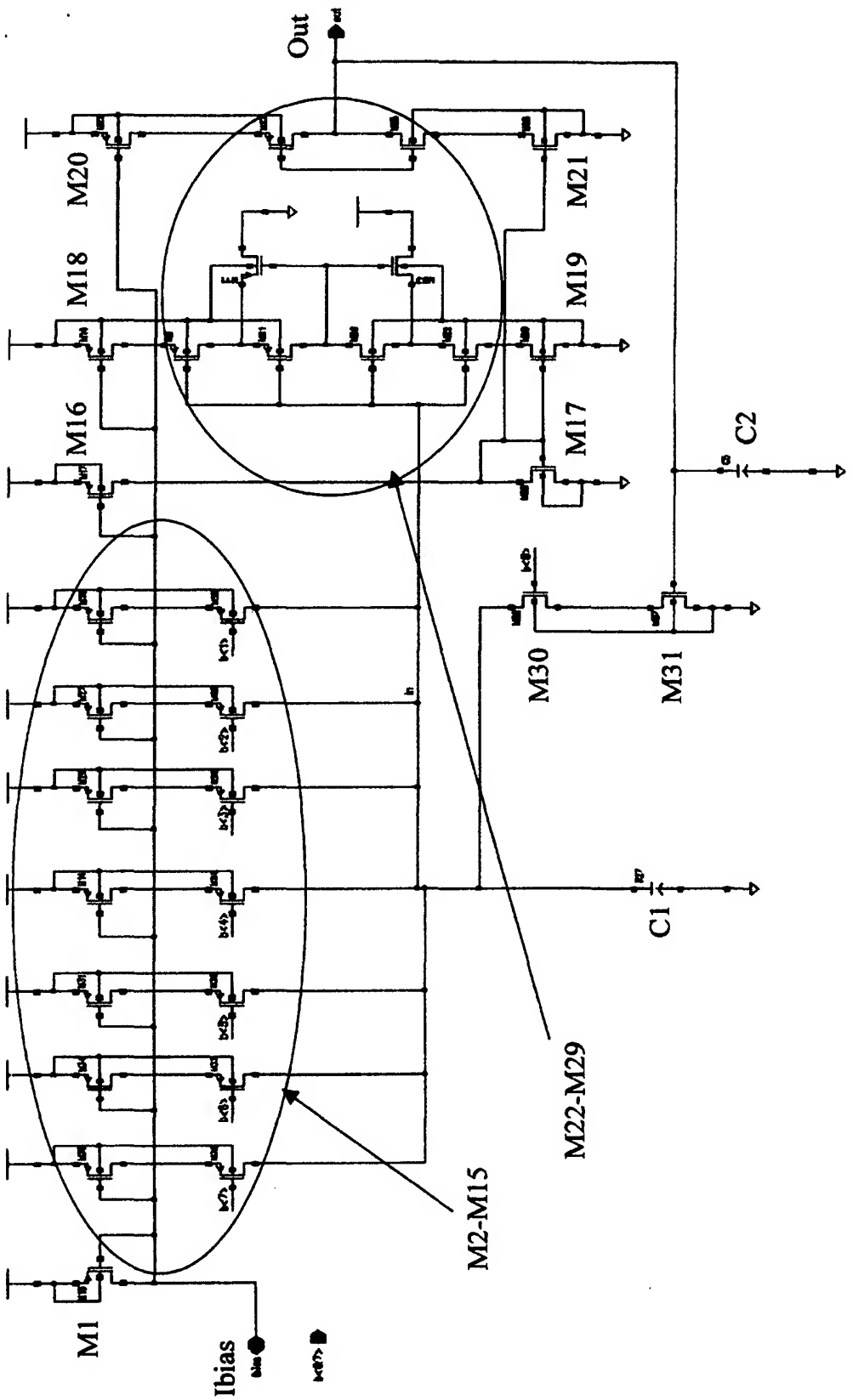

Figure 2

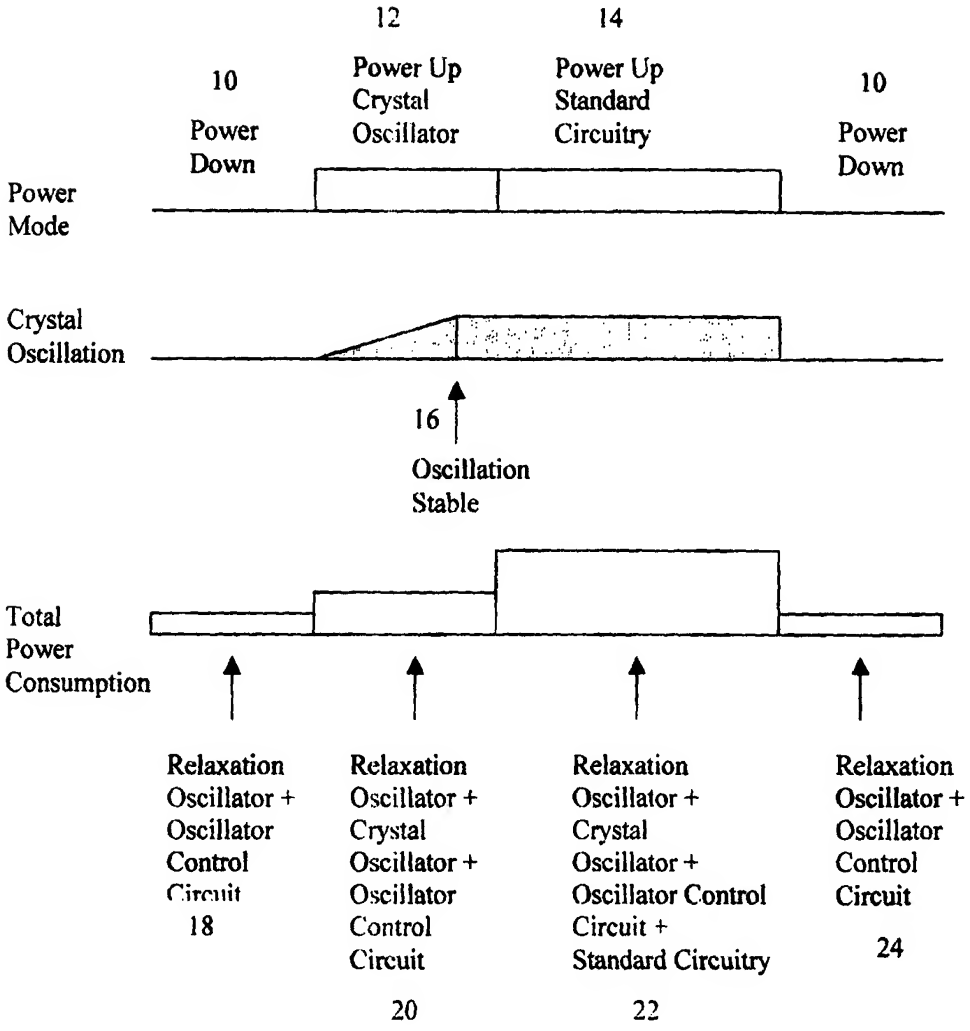
12
14
10
Power Up Crystal Oscillator
Power Up Standard Circuitry
10
Power Down
Power Down
Power Mode
Crystal Oscillation
16
Oscillation Stable
Total Power Consumption
Relaxation Oscillator + Oscillator Control Circuit
18
Relaxation Oscillator + Crystal Oscillator + Oscillator Control Circuit
20
Relaxation Oscillator + Crystal Oscillator + Oscillator Control Circuit + Standard Circuitry
22
Relaxation Oscillator + Oscillator Control Circuit
24

Figure 3

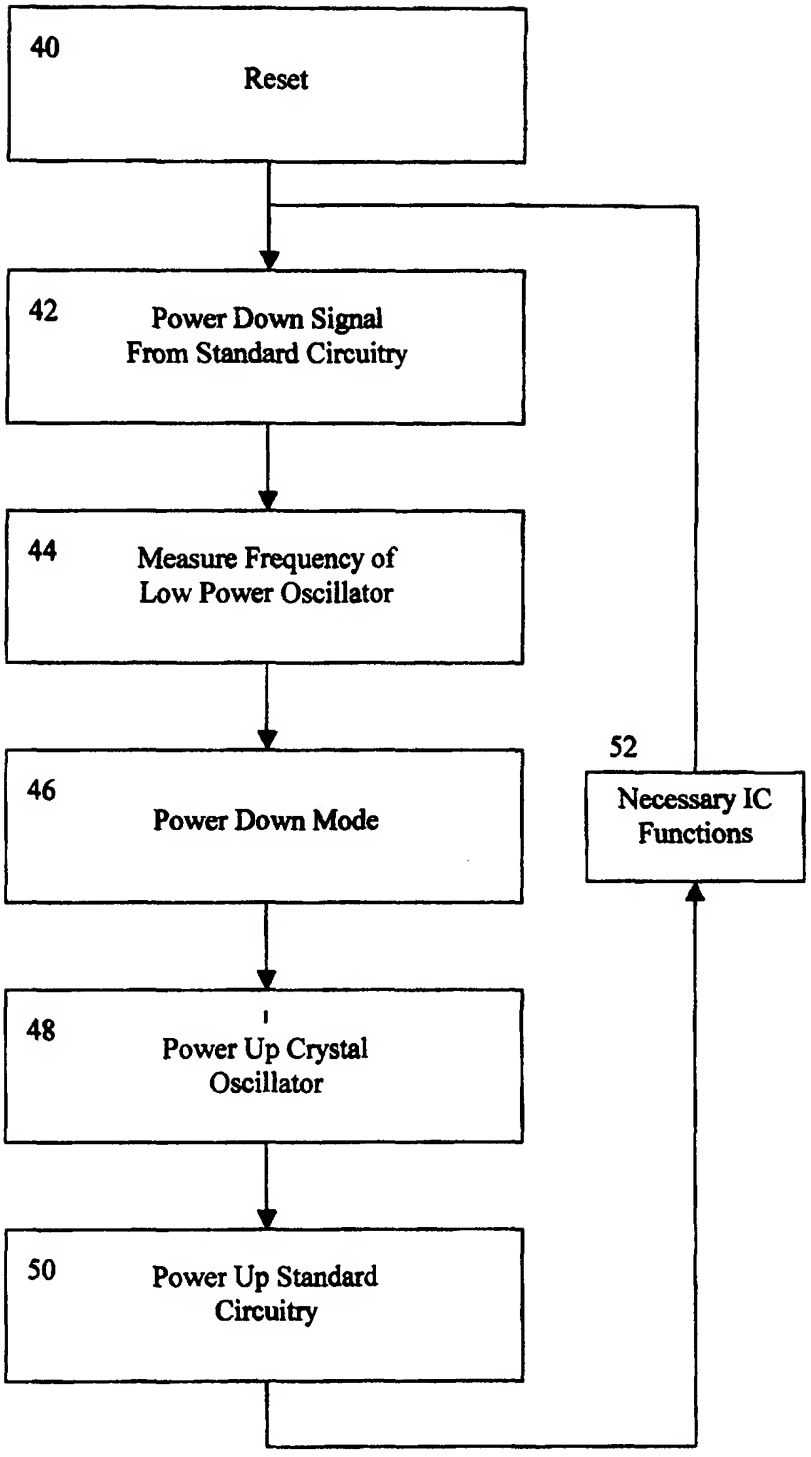
40
Reset
42
Power Down Signal From Standard Circuitry
44
Measure Frequency of Low Power Oscillator
46
Power Down Mode
48
Power Up Crystal Oscillator
50
Power Up Standard Circuitry
52
Necessary IC Functions

Figure 4